Paulo Isagani M. Urriza

pmurriza@ucla.edu
Tel: +1 213 309 3667
2200 Monroe St Apt 1105, Santa Clara, CA 95050-3439, USA
paulourriza.com

Summary

- 5+ years systems and algorithm design experience for Analog/DSP-based SerDes IP (from 12G-112G)
- Key designer on several generations of multi-rate, multi-standard SerDes IP utilized in most of the Marvell SoC portfolio (Storage, PHY, and Switch SOCs: PCIe3-5, SAS, IEEE and OIF standards for chip-to-chip, VSR, backplane, copper)
- Strong background on wired/wireless communication theory and DSP algorithm design

Technical Skills

- *Programming:* MATLAB/Simulink, C/C++ (general purpose/FW development), Python, Unix shell scripting, Xilinx SysGen, HDL basics (Verilog, VHDL, SystemC), Version Control (Git/SVN)
- *Hardware Platforms:* Marvell Raptor/CAP2 (Automation Platform), Universal Software Radio Platform (USRP), Berkeley Emulation Engine (BEE2-Virtex4)

Work Experience

Marvell Semiconductor

- Senior Manager, DSP 05/19–12/19
  - Technical lead of a small team (6 DSP engineers) in addition to individual contributor role
  - Developed a Python-based scripting framework for prototyping SerDes training/adaptation algorithms that can be tested directly on silicon (used as reference by FW designers, verification, and for lab testing/validation)
  - Primary system architect / algorithm designer for Marvell's analog-based PAM4 SerDes solutions (56G and 112G)
- Senior System Engineer, Staff System Engineer 07/14–05/19
  - Key system architect/designer of Marvell's multi-standard (SAS, PCIE3-5, IEEE, OIF) SerDes from 28G (NRZ), 56G (PAM4), up to 112G (both analog and ADC-based solutions)
  - Lead designer/developer of training algorithm used in Marvell's Analog-based 56G-112G SerDes
  - Developed a MATLAB-based SerDes performance evaluation tool (both statistical and time-domain)
  - Developed C++ Simulator/Model used for performance evaluation, architecture exploration, and digital verification (bit-match) for several SerDes generations
  - Contributed in various capacities to SerDes IP development including
    * Digital verification (C++ models, debugging, scripting for regression tests)
    * CDR analysis (modeling, evaluation)
    * Tx-Train and Rx-Train algorithm development
    * Delivered specifications for equalization and adaptation of analog SerDes IP
    * Leading multi-team collaboration (DSP, Digital, Analog, Applications Engineering)
    * Chip bring-up, lab validation, and test plan delivery/execution

UCLA, Department of Electrical Engineering

- Graduate Student Researcher, Teaching Assistant 09/09–06/14
  - Taught undergraduate discussion classes in Digital Logic Design
  - Research focusing on techniques for detecting, localizing and identifying transmitters for Cognitive Radio applications

University of the Philippines, Electrical and Electronics Engineering Institute (EEEI)

- Teaching Associate 06/07–05/09
  - Taught undergraduate discussion/lab classes in Signals and Systems, Digital Logic Design, Electromagnetics, Probability Theory

Education

Ph.D. Electrical Engineering (Signals and Systems Track) 09/09–06/14

- University of California Los Angeles (UCLA)
- *Adviser:* Prof. Danijela Čabrić, Ph.D.
- *Affiliation:* UCLA Cognitive and Reconfigurable Embedded Systems Laboratory (CORES Lab)
- *Dissertation Title:* "Advanced Spectrum Sensing for Multiple Transmitter Identification"

M.S. Electrical Engineering 06/07–08/09

- University of the Philippines Diliman
- *Adviser:* Prof. Joel Joseph S. Marciano, Jr. Ph.D.
- *Affiliation:* University of the Philippines Digital Signal Processing Lab
- *Thesis:* "Parallel Sequence Spread Spectrum - OFDM (PSSS-OFDM) Scheme - A Novel Physical Layer Scheme for Robust Wireless Communication Systems"

B.S. Computer Engineering 06/02–04/07

- University of the Philippines Diliman
- Magna Cum Laude, Rank **1 out of 55** in Computer Engineering, **4 out of 820** in Engineering
- Ranked within top **50 out of** $\sim$**70,000** in nationwide college entrance exam (UPCAT), UP Oblation Scholar

Research Experience

DARPA-CLASIC – Analog-FFT based Cognitive Radio Sensor IC

- Developed several signal processing algorithms for blind modulation classification.
- Developed a full real-time modulation classification system.
- Experimental verification using Universal Software Radio Platform (USRP) and FPGA platforms.
- Development using the Xilinx System Generator with the Berkeley Emulation Engine (BEE2)

COgnitive and Reconfigurable Embedded Systems (CORES) Lab

- MAC Scheme Classification – Classification of upper layer schemes employed by unknown transmitters
- Multiple Antenna Cyclostationary Spectrum Sensing – algorithm development and mathematical analysis of a multiple-sensor feature-based spectrum sensing system.
- Localization Techniques for Cognitive Radios – Mathematical analysis of range-free localization techniques for CR applications. Developed and simulated a distributed algorithm for range-free localization.

Wireless Communications Engineering Laboratory (WCEL)

- Algorithm development for PHY layer techniques based on spread spectrum and OFDM and subsequent implementation on a FPGA-based rapid-prototyping platform.

Digital Signal Processing Laboratory (DSP Lab)

- Senior project focusing on hardware implementation of space-time coding and other MIMO techniques on an FPGA platform using VHDL.

Publications

Journals, Letters and Magazines

- **P. Urriza**, E. Rebeiz, and D. Čabrić, *"Optimal Discriminant Functions Based on Sampled Distribution Distance for Modulation Classification"*, IEEE Communications Letters, vol.17, no.10, pp.1885-1888, August 2013.
- **P. Urriza**, E. Rebeiz, and D. Čabrić, *"Multiple Antenna Cyclostationary Spectrum Sensing Based on the Cylic Correlation Significance Test"*, IEEE Journal on Selected Areas in Communications, vol.31, no.11, pp.2185-2195, October 2013.
- **P. Urriza**, E. Rebeiz, P. Pawełczak, and D. Čabrić, *"Computationally Efficient Modulation Level Classification Based on Probability Distribution Distance Functions"*, IEEE Communications Letters, vol.15, no.5, pp.476-478, May 2011.
- M. Laghate, **P. Urriza**, and D. Čabrić, *"Channel Access Method Classification for Cognitive Radio Applications"*, IEEE Wireless Communications Letters, vol.7, no.1, pp.70-73, February 2018.
- E. Rebeiz, F-L. Yuan, **P. Urriza**, D. Marcović, and D. Čabrić, *"Energy-Efficient Processor for Blind Signal Classification in Cognitive Radio Networks"*, IEEE Transactions on Circuits and Systems I: Regular Papers, vol.61, no.2, pp.587-599, February 2014.
- E. Rebeiz, **P. Urriza**, and D. Čabrić, *"Optimizing Wideband Cyclostationary Spectrum Sensing under Receiver Impairments"*, IEEE Transactions on Signal Processing, vol.61, no.15, pp.3931-3943, August 2013.
- J. Wang, **P. Urriza**, Y. Han, and D. Čabrić, *"Weighted Centroid Algorithm for Estimating Primary User Location: Theoretical Analysis and Distributed Implementation"*, IEEE Transaction on Wireless Communications, vol.10, no.10, pp.3403-3413, October 2011.

Conferences

- **P. Urriza**, E. Rebeiz, and D. Čabrić, *"Eigenvalue-based Cyclostationary Spectrum Sensing Using Multiple Antennas"*, in Proc. IEEE GLOBECOM. Anaheim, CA, USA, 3-7 Dec. 2012.
- **P. Urriza**, E. Rebeiz, and D. Čabrić, *"Hardware Implementation of Kuiper-based Modulation Level Classification"*, in Proc. Asilomar Conference on Signals, Systems, and Computers. Pacific Grove, CA, USA, 6-9 Nov. 2011.
- **P. Urriza**, and J. Marciano, *"Combining Parallel Sequence Spread Spectrum (PSSS) with OFDM - Concept and Simulation Results"*, in Proc. IEEE WCNC. Sydney, Australia, 18-21 Apr. 2010.
- E. Rebeiz, **P. Urriza**, and D. Čabrić, *"Experimental Analysis of Cyclostationary Detectors Under Cyclic Frequency Offsets"*, in Proc. Asilomar Conference on Signals, Systems, and Computers. Pacific Grove, CA, USA, 4-7 Nov. 2012.
- J. Wang, **P. Urriza**, Y. Han, and D. Čabrić, *"Performance Analysis of Weighted Centroid Algorithm for Primary User Localization in Cognitive Radio Networks"*, in Proc. Asilomar Conference on Signals, Systems, and Computers. Pacific Grove, CA, USA, 7-10 Nov. 2010.
- G. Fadera, L. Ignacio, M. Nastor, **P. Urriza**, and J. Marciano, *"FPGA implementation of space-time encoders"*, in Proc. Intelligent and Advanced Systems. Kuala Lumpur, Malaysia, 25-28 Nov. 2007.

Grants and Awards

- Qualcomm Cognitive Radio Competition - *Member, UCLA CORES team ranked within the Top 3 Finalists*
- Dept. of Science and Technology (DOST)[1] Accelerated Human Resource Development Program Scholar (MS EE), 2007-2009 - *Merit-based scholarship for a Masters in the field of science or engineering*
- UP Oblation Scholarship Award - Top **50 out of** ∼**70,000** in the University of the Philippines College Entrance Test - *Nationwide aptitude test*

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`http://paulourriza.com`

[1] DOST - Philippine Gov't Agency corresponding to the NSF in USA